**I M.Sc Phyiscs**

**ANALOG ELECTRONICS, MICROPROCESSORS AND MICROCONTROLLER**

**UNIT I : ANALOG CIRCUITS**

1). Op-Amp is abbreviated as \_\_\_\_\_\_\_\_.

a) Operational Amplifier

b) Operand amplitude

c) Operational amplitude

d) None of the above

Ans: a

2). Op-Amp is a \_\_\_\_\_\_ type of amplifier.

a) Current

b) Voltage

c) Power

d) Resistance

Ans: b

3). Op-Amp is \_\_\_\_\_\_ coupled voltage type of amplifier.

1. AC
2. DC
3. ADC
4. DAC

Ans: b

4). Op-Amp has \_\_\_\_\_\_\_ gain.

1. High
2. Low
3. Zero
4. Medium

Ans : a

5). A device with direct current coupled, high gain electronic voltage type amplifier with one output and differential input is called \_\_\_\_\_\_.

1. Rectifier
2. Amplifier
3. Transformer
4. Op-amp

Ans : d

6). Op-Amp has \_\_\_\_\_\_\_\_ inputs.

1. Single
2. Similar
3. Zero
4. Differential

Ans: d

7). Op-Amp has \_\_\_\_\_\_\_\_ outputs.

1. Single
2. Similar
3. Multiple
4. Differential
5. Ans: a

8). The potential output of Op-Amp is \_\_\_\_\_ times greater than the potential difference of input.

1. 100 times
2. 10000 times
3. 100,000 times
4. 10000000 times

Ans: c

9). Op-Amp is originated from \_\_\_\_\_\_\_\_ computers.

1. Analog
2. Digital
3. Both a and b
4. None of the above

Ans: a

10). Op-Amp performs \_\_\_\_\_\_\_\_ operations.

1. Arithmetic
2. Logical
3. Alphanumeric
4. Both a and b

Ans: d

11). Op-Amp performs which type of mathematical type operations.

1. Linear
2. Non-linear
3. Frequency-dependent
4. All the above

Ans; d

12). Op-Amp was invented by \_\_\_\_\_\_\_\_**.**

1. Henry
2. Richard
3. Karl D
4. David

Ans: c

13). Op-Amp was invented by Karl D in which year?

1. 1966
2. 1967
3. 1968
4. 1999

Ans: b

14). Op-Amp has \_\_\_\_\_\_ input type configuration.

1. 2
2. 3
3. 4
4. 5

Ans: a

15). Op-Amp with positive input type configuration is represented as \_\_\_\_\_\_\_.

1. +V
2. -V
3. V
4. Both a and c

Ans: d

16). Op-Amp with negative input type configuration is represented as \_\_\_\_\_\_\_.

1. +V
2. -V
3. V
4. Both a and c

Ans: b

17). Op-Amp with positive input type configuration +V or V is called \_\_\_\_\_\_\_.

1. Non-inverting type input
2. Inverting type input
3. Non-inverting type output
4. Inverting type output

Ans: a

18). Op-Amp with negative input type configuration -V is called \_\_\_\_\_\_\_.

1. Non-inverting type input
2. Inverting type input
3. Non-inverting type output
4. Inverting type output

Ans: b

19). Op-amp output is represented as \_\_\_\_\_\_\_.

1. Vin
2. Vout
3. V+
4. V-

Ans: b

20). Op-Amp has how many terminals?

1. 2
2. 3
3. 4
4. 5

Ans: d

21). +Vs is also called as \_\_\_\_\_\_\_\_.

1. Positive power supply
2. Negative power supply
3. Both a and b
4. Power supply

Ans:a

22). -Vs is also called \_\_\_\_\_\_\_\_.

1. Positive power supply
2. Negative power supply
3. Both a and b
4. Power supply

Ans: b

23). An op-amp with negative feedback provides \_\_\_\_\_ output parameter.

1. Gain
2. Bandwidth
3. Input-output impedance
4. All the above

Ans: c

24). Balancing type feedback is also called as \_\_\_\_\_\_**\_.**

1. Positive type feedback
2. Negative type feedback
3. Both a and b
4. None of the above

 Ans: b

25). Which of the following are the examples of negative feedback?

1. Mercury thermostats
2. Centrifugal governors
3. Steering engine
4. All the above

Ans: d

26. A differential amplifier ………..

1. is a part of an OP-amp
2. has one input and one output
3. both
4. none of the above

Answer: c) both

27. When a differential amplifier is operated single-ended, …………..

1. the output is grounded
2. one input is grounded and signal is applied to the other
3. both inputs are connected together
4. the output is not inverted

**Answer:  b**

28. In differential-mode, …………..

1. opposite polarity signals are applied to the inputs
2. the gain is one
3. the outputs are of different amplitudes
4. only one supply voltage is used

**Answer: a**

29. In the common-mode, …………..

1. both inputs are grounded
2. the outputs are connected together
3. an identical signal appears on both inputs
4. the output signals are in-phase

**Answer: c**

**30**. The common-mode gain is ….

1. very high
2. very low
3. always unity
4. unpredictable

**Answer: b**

31. The differential gain is ….

1. very high
2. very low
3. dependent on input voltage
4. about 100

**Answer: a**

32. If *ADM* = 3500 and *ACM* = 0.35, the CMRR is ….

1. 1225
2. 10,000
3. 80 dB
4. 10,000 & 80 dB

**Answer: d**

33. With zero volts on both inputs, an OP-amp ideally should have an output ….

1. equal to the positive supply voltage
2. equal to the negative supply voltage
3. equal to zero
4. equal to the CMRR

**Answer: c**

34. Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is ….

1. 1
2. 2000
3. 80 dB
4. 100,000

**Answer: d**

35. A certain OP-amp has bias currents of 50 μA and 49.3 μA. The input offset current is ….

1. 700 nA
2. 99.3 μA
3. 49.7 μA
4. none of these

**Answer: a**

36. The output of a particular OP-amp increases 8 V in 12 μs. The slew rate is ….

1. 90 V/μs
2. 0.67 V/μs
3. 1.5 V/μs
4. none of these

**Answer:b**

**3**7.For an OP-amp with negative feedback, the output is ….

1. equal to the input
2. increased
3. feed back to the inverting input
4. feed back to the noninverting input

Ans : b

38. The use of negative feedback ….

1. reduces the voltage gain of an OP-amp
2. makes linear operation possible
3. both
4. none of the above

**Answer: c**

39. Negative feedback ….

1. increases the input and output impedances
2. increases the input impedance and bandwidth
3. decreases the output impedance and bandwidth
4. does not affect impedance or bandwidth

**Answer: b**

40. A certain noninverting amplifier has *Ri* of 1 kΩ and *Rf* of 100 kΩ. The closed-loop voltage gain is ….

1. 100,000
2. 1000
3. 101
4. 100

**Answer: c**

41. If feedback resistor in Q.15 is open, the voltage gain ……………

1. increases
2. decreases
3. is not affected
4. depends on Ri

**Answer: a**

42. A certain inverting amplifier has a closed-loop voltage gain of 25. The OP-amp has an open-loop voltage gain of 100,000. If an OP-amp with an open-loop voltage gain of 200,000 is substituted in the arrangement, the closed-loop gain ……….

1. doubles
2. drops to 12.5
3. remains at 25
4. increases slightly

**Answer: c**

43. voltage follower ….

1. has a voltage gain of 1
2. in noninverting
3. has no feedback resistor
4. has all of these

**Answer: a**

44. The OP-amp can amplify ….

1. a.c. signals only
2. d.c. signals only
3. both a.c. and d.c. signals
4. neither d.c. nor a.c. signals

**Answer: c**

45. The input offset current equals the ….

1. difference between two base currents
2. average of two base currents
3. collector current divided by current gain
4. none of these

**Answer: a**

46. The tail current of a differential amplifier is ….

1. half of either collector current
2. equal to either collector current
3. two times either collector current
4. equal to the difference in base currents

**Answer: c**

47. The node voltage at the top of the tail resistor is closest to ….

1. collector supply voltage
2. zero
3. emitter supply voltage
4. tail current times base resistance

**Answer:  b**

48. The tail current in a differential amplifier equals ….

1. difference between two emitter currents
2. sum of two emitter currents
3. collector current divided by current gain
4. collector voltage divided by collector resistance

**Answer: b**

49. The differential voltage gain of a differential amplifier is equal to RC divided by ….

1. r′e
2. r′e/2
3. 2 r′e
4. *RE*

**Answer: c**

50. The input impedance of a differential amplifier equals r′e times ….

1. β
2. *RE*
3. *RC*
4. 2β

**Answer: d**

51. A common-mode signal is applied to ….

1. the noninverting input
2. the inverting input
3. both inputs
4. top of the tail resistor

**Answer: c**

52. The common-mode voltage gain is ….

1. smaller than differential voltage gain
2. equal to differential voltage gain
3. greater than differential voltage gain
4. none of the above

**Answer: a**

53. The input stage of an OP-amp is usually a ….

1. differential amplifier
2. class B push-pull amplifier
3. CE amplifier
4. swamped amplifier

**Answer: a**

54. The common-mode voltage gain of a differential amplifier is equal to RC divided by ….

1. r′e
2. 2 r′e
3. r′e /2
4. 2 RE

**Answer: d**

55. Current cannot flow to ground through ….

1. a mechanical ground
2. an a.c. ground
3. a virtual ground
4. an ordinary ground

**Answer: c**

56. Operational Amplifier consists of the following features  \_\_\_\_\_\_\_\_\_\_\_\_\_\_.

1. Very High Gain
2. Very High Input Impedance
3. Very Low Output Impedance
4. all are correct

**Answer: d**

57. Today OP AMP are made with the help of  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

1. Discrete devices
2. Integrated Circuits
3. Vacuum Tubes
4. a & c are correct

**Answer: b**

58. When the feedback not applied to the OP Amplifier then it works as \_\_\_\_\_\_\_.

1. Open Loop Mode
2. Closed Loop Mode
3. Variable Loop Mode
4. Negative Loop Mode

Answer: a

59. When the feedback is applied to the OP Amplifier then it works as \_\_\_\_\_\_\_.

1. Open Loop Mode
2. Closed Loop Mode
3. Variable Loop Mode
4. Negative Loop Mode

**Answer: b**

60. Operational AMP is available in the packages of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. DIP
2. To-5 Case
3. Flat Pack
4. All are correct

**Answer: d**

**UNIT.II – MICROPROCESSOR -8085**

 1. 8085 microprocessor is an 8-bit microprocessor designed by?

1. IBM
2. Dell
3. Intel
4. VAX

Ans: c

 2. In 8085, 16-bit address bus, which can address upto?

1. 16KB
2. 32KB
3. 64KB
4. 128KB

Ans:c

 3. There are \_\_\_\_\_\_\_ general purpose registers in 8085 processor

1. 5
2. 6
3. 7
4. 8

Ans: b

 4. It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.

1. Flag register
2. Stack pointer
3. Temporary register
4. Program counter

Ans: a

 5. Flag register is an 8-bit register having

1. It is an 8-bit register, which holds the temporary data of arithmetic and logical operations.
2. When an instruction is fetched from memory then it is stored in the program counter
3. It provides timing and control signal to the microprocessor
4. It is a 16-bit register used to store the memory address location of the next instruction to be executed.

Ans: d

6. A set of register which contain are

1. data
2. memory address
3. result
4. all of these

Ans: d

 7. This signal indicates that another master is requesting the use of the address and data buses.

1. READY
2. HOLD
3. HLDA
4. INTA

Ans: b

 8. This signal is used as the system clock for devices connected with the microprocessor.

1. X1, X2
2. CLK OUT
3. CLK IN
4. IO/M

Ans: b

 9. Which of the following is true about Control and status signals?

1. These signals are used to identify the nature of operation.
2. There are 3 control signal and 3 status signals.
3. Three status signals are IO/M, S0 & S1.
4. All of the above

Ans: d

 10. MVI K, 20F is an example of?

1. Register addressing mode
2. Direct addressing mode
3. Immediate addressing mode
4. Indirect addressing mode

Ans: a

11) What is Microprocessor?
a) A multipurpose PLD that accepts binary data as input
b) A multipurpose PLD that accepts an integer as input
c) A multipurpose PLD that accepts whole numbers as input
d) A multipurpose PLD that accepts prime numbers as input

Ans: a

12) Which of the following is a type of microprocessor?
a) CISC
b) RISC
c) EPIC
d) All of the mentioned

Ans: d

13) The microprocessor of a computer can operate on any information if it is present in \_\_\_\_\_\_\_\_\_\_\_\_\_\_ only.
a) Program Counter
b) Flag
c) Main Memory
d) Secondary Memory

Ans: d

14) Which of the following technology was used by Intel to design its first 8-bit microprocessor?
a) NMOS
b) HMOS
c) PMOS
d) TTL

Ans: c

15) What is the word length of an 8-bit microprocessor?
a) 8-bits – 64 bits
b) 4-bits – 32 bits
c) 8-bits – 16 bits
d) 8-bits – 32 bits

Ans: a

16) In 8-bit microprocessor, how many opcodes are present?
a) 246
b) 278
c) 250
d) 256

Ans: a

17) Which of the following is not true about the address bus?
a) It consists of control PIN 21 to 28
b) It is a bidirectional bus
c) It is 16 bits in length
d) Lower address bus lines (AD0 – AD7) are called “Line number”

Ans: b

18) Which of the following is true about microprocessors?
a) It has an internal memory
b) It has interfacing circuits
c) It contains ALU, CU, and registers
d) It uses Harvard architecture

Ans: c

19) Which of the following is the correct sequence of operations in a microprocessor?
a**)** Opcode fetch, memory read, memory write, I/O read, I/O write
b) Opcode fetch, memory write, memory read, I/O read, I/O write
c) I/O read, opcode fetch, memory read, memory write, I/O write
d) I/O read, opcode fetch, memory write, memory read, I/O write

Ans: a

20) The \_\_\_\_\_\_\_\_ directive instructs the assembler to begin memory allocation for a segment/block/code from the stated address.
a) GROUP
b) OFFSET
c) ORG
d) LABEL

Ans: c

21) Which of the following is not a microprocessor?
a) Z8000
b) Motorola 6809
c) Zilog Z8
d) PIC1x

Ans: d

22) Which of the following is not a property of TRAP interrupt in microprocessor?
a) It is a non-maskable interrupt
b) It is of highest priority
c) It uses edge-triggered signal
d) It is a vectored interrupt

Ans: c

23) Which of the following is a property of RST 7.5 interrupt?
a) It is a non-maskable interrupt
b) It has 3rd highest priority
c) It uses level-triggered signal
d) Its vectored address is 0034H

Ans: d

24) Which of the following flag is used to mask INTR interrupt?
a) zero flag
b) auxiliary carry flag flag
c) interrupt flag
d) sign flag

Ans: c

25) Which of the following is a special-purpose register of microprocessor?
a) Program counter
b) Instruction register
c) Accumulator
d) Temporary register

Ans: a

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d) A multipurpose PLD that accepts prime numbers as input

Answer: a

27)Which of the following is correct about 8086 microprocessor?
a) Intel’s first x86 processor
b) Motrola’s first x86 processor
c) STMICROELECTRONICS’s first x86 processor
d) NanoXplore x86 processor

Answer: a

28) Which of the following is a type of microprocessor?
a) CISC
b) RISC
c) EPIC
d) All of the mentioned

Answer: d

29)The microprocessor of a computer can operate on any information if it is present in \_\_\_\_\_\_\_\_\_\_\_\_\_\_ only.
a) Program Counter
b) Flag
c) Main Memory
d) Secondary Memory

Answer: c.

30). Which of the following technology was used by Intel to design its first 8-bit microprocessor?
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c) PMOS
d) TTL

Answer: c

31) Which of the following addressing method does the instruction, MOV AX,[BX] represent?
a) register indirect addressing mode
b) direct addressing mode
c) register addressing mode
d) register relative addressing mode

Answer: a

32). What is the word length of an 8-bit microprocessor?
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b) 4-bits – 32 bits
c) 8-bits – 16 bits
d) 8-bits – 32 bits

Answer: a

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a) 246
b) 278
c) 250
d) 256
Answer: a.

34). Which of the following is not true about the address bus?
a) It consists of control PIN 21 to 28
b) It is a bidirectional bus
c) It is 16 bits in length
d) Lower address bus lines (AD0 – AD7) are called “Line number”
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a) It has an internal memory
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a) Opcode fetch, memory read, memory write, I/O read, I/O write
b) Opcode fetch, memory write, memory read, I/O read, I/O write
c) I/O read, opcode fetch, memory read, memory write, I/O write
d) I/O read, opcode fetch, memory write, memory read, I/O write

Answer: a

37). The \_\_\_\_\_\_\_\_ directive instructs the assembler to begin memory allocation for a segment/block/code from the stated address.
a) GROUP
b) OFFSET
c) ORG
d) LABEL
Answer: c

38).The location counter is initialized to 0000H if the directive is not present.

13. Which of the following is not a microprocessor?
a) Z8000
b) Motorola 6809
c) Zilog Z8
d) PIC1x
Answer: d

39). Which of the following is not a property of TRAP interrupt in microprocessor?
a) It is a non-maskable interrupt
b) It is of highest priority
c) It uses edge-triggered signal
d) It is a vectored interrupt
Answer: c

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d) Its vectored address is 0034H

Answer: d

41). Which of the following flag is used to mask INTR interrupt?
a) zero flag
b) auxiliary carry flag flag
c) interrupt flag
d) sign flag
Answer: c

42) Which of the following is a special-purpose register of microprocessor?
a) Program counter
b) Instruction register
c) Accumulator
d) Temporary register
Answer: a

43). Which of the following circuit is used as a special signal to demultiplex the address bus and data bus?
a) Priority Encoder
b) Decoder
c) Address Latch Enable
d) Demultiplexer
Answer: c

44). How many flip-flops are there in a flag register of 8085 microprocessor?
a) 4
b) 5
c) 7
d) 10
Answer: b

45). Which of the following flag condition is used for BCD arithmetic operations in microprocessor?
a) Sign flag
b) Auxiliary carry flag
c) Parity flag
d) Zero flag
Answer: b

46). Whenever a non-maskable interrupt occurs in 8085 microprocessor, which of the following data line contains the data?
a) 2C H
b) 3C H
c) 36 H
d) 24 H
Answer: d

47). What does a microprocessor understand after decoding opcode?
a) Perform ALU operation
b) Go to memory
c) Length of the instruction and number of operations
d) Go to the output device
Answer: c

48). How many address lines are present in 8086 microprocessor?
a) 16
b) 20
c) 32
d) 40
Answer: b

49). Which of the following is not a status flag in microprocessor?
a) Overflow flag
b) Direction flag
c) Interrupt flag
d) Index flag
Answer: d

50). Which of the following is not a condition flag?
a) Trap flag
b) Auxiliary carry flag
c) Parity flag
d) Zero flag
Answer: a

51). Which of the following register is not used in opcode fetch operations?
a) Program counter
b) Memory address register
c) Memory data register
d) Flag register
Answer: d

52). A memory connected to a microprocessor has 20 address lines and 16 data lines. What will be the memory capacity?
a) 8 KB
b) 2 MB
c) 16 MB
d) 64 KB
Answer: b

53). What is the word length of the Pentium-II microprocessor?
a) 8-bit
b) 32-bit
c) 64-bit
d) 16-bit
Answer: c

54). Which of the following is not true about 8085 microprocessor?
a) It is an 8-bit microprocessor
b) It is a 40 pin DIP chip
c) It is manufactured using PMOS technology
d) It has 16 address lines
Answer: c

55). Which of the following is a non-vectored input?
a) TRAP
b) RST-7.5
c) RST-6.5
d) INTR
Answer: d

56). Which of the following is true?
a) Every instruction has two parts i.e. opcode and operands
b) MOV B, C is a two-byte instruction
c) MVI A, 90H is a three-byte instruction
d) Maximum number of T-states possible for the execution of an instruction is 16
Answer: a

57). Which of the following addressing mode is used by 8085 microprocessor for array and list operations?
a) Base-Register
b) Direst
c) Indexed
d) Immediate
Answer: c

58). What is stored in the H & L general-purpose register?
a) Opcode
b) Address of memory
c) Address of next instruction
d) Temporary data
Answer: b

59). If a 90 GB memory has to be connected to a microprocessor, minimum how many address lines are required?
a) 36
b) 39
c) 32
d) 37
Answer: d

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60). Which of the following is a software interrupt?
a) TRAP
b) INTR
c) RST-6.5
d) RST-5
Answer: d

**Unit – III Microprocessor-8086**

1. A microprocessor is a chip integrating all the functions of a CPU of a computer.
	1. multiple B. single C. double D. triple ANSWER: B
2. Microprocessor is a/an circuit that functions as the CPU of the compute
	1. electronic B. mechanic C. integrating D. processing ANSWER: A
3. Microprocessor is the of the computer and it perform all the computational tasks
	1. main B. heart C. important D. simple ANSWER: B
4. The intel 8086 microprocessor is a processor
	1. 8 bit B. 16 bit C. 32 bit D. 4 bit ANSWER: B
5. The microprocessor can read/write 16 bit data from or to
	1. memory B. I /O device C. processor D. register ANSWER: A
6. In 8086 microprocessor , the address bus is bit wide

 A. 12 bit B. 10 bit C. 16 bit D. 20 bit ANSWER: D

1. The work of EU is
	1. encoding B. decoding C. processing D. calculations ANSWER: B
2. The 16 bit flag of 8086 microprocessor is responsible to indicate
	1. the condition of result of ALU operation B. the condition of memory

C. the result of addition D. the result of subtraction ANSWER: A

1. The CF is known as
	1. carry flag B. condition flag C. common flag D. single flag

.ANSWER: A

1. The register AX is formed by grouping
	1. AH & AL B. BH & BL C. CH & CL D. DH & DL ANSWER: A
2. The BP is indicated by
	1. base pointer B. binary pointer C. bit pointer D. digital pointer ANSWER: A
3. The index register are used to hold
	1. memory register B. offset address C. segment memory D. offset memory ANSWER: A
4. The BIU prefetches the instruction from memory and store them in
	1. queue B. register C. memory D. stack

ANSWER: A

1. The JS is called as
	1. jump the signed bit B. jump single bit

C. jump simple bit D. jump signal it ANSWER: A

1. The microprocessor determines whether the specified condition exists or not by testing the
	1. carry flag B. conditional flag C. common flag D. sign flag ANSWER: B
2. The 8086 fetches instruction one after another from of memory
	1. code segment B. IP C. ES D. SS ANSWER: A
3. The BIU contains FIFO register of size 6 bytes called .
	1. queue B. stack C. segment D. register ANSWER: A
4. The pin of minimum mode AD0-AD15 has address
	1. 16 bit B. 20 bit C. 32 bit D. 4 bit ANSWER: B
5. The address bits are sent out on lines through

A. A16-19 B. A0-17 C. D0-D17 D. C0-C17 ANSWER: A

1. is used to write into memory
	1. RD B. WR C. RD / WR D. CLK ANSWER: B
2. The RD, WR, M/IO is the heart of control for a mode
	1. minimum B. maximum C. compatibility mode D. control mode ANSWER: A
3. If MN/MX is low the 8086 operates in mode
	1. Minimum B. Maximum C. both (A) and (B) D. medium ANSWER: B
4. In max mode, control bus signal So,S1 and S2 are sent out in form
	1. decoded B. encoded C. shared D. unshared ANSWER: B
5. The main concerns of the are to define a flexible set of commands
	1. memory interface B. peripheral interface

C. both (A) and (B) D. control interface

.ANSWER: A

1. Primary function of memory interfacing is that the should be able to read from and write into register
	1. multiprocessor B. microprocessor C. dual Processor D. coprocessor ANSWER: B
2. signal is generated by combining RD and WR signals with IO/M

A. control B. memory C. register D. system ANSWER: A

1. The primary function of the is to accept data from I/P devices
	1. multiprocessor B. microprocessor C. peripherals D. interfaces ANSWER: B
2. signal prevent the microprocessor from reading the same data more than one
	1. pipelining B. handshaking C. controlling D. signaling ANSWER: B
3. The pin is used to select direct command word
	1. A0 B. D7-D6 C. A12 D. AD7-AD6 ANSWER: A
4. In which year, 8086 was introduced?

A. 1978 B. 1979 C. 1977 D. 1981 ANSWER: A

1. Expansion for HMOS technology\_
	1. high level mode oxygen semiconductor
	2. high level metal oxygen semiconductor
	3. high performance medium oxide semiconductor
	4. high performance metal oxide semiconductor ANSWER: D
2. In 8086 the overflow flag is set when .
	1. the sum is more than 16 bits.
	2. signed numbers go out of their range after an arithmetic operation.
	3. carry and sign flags are set.
	4. subtraction ANSWER: B
3. In 8086 microprocessor one of the following statements is not true?
	1. coprocessor is interfaced in max mode. B. coprocessor is interfaced in min mode.

C. I /O can be interfaced in max / min mode. D. supports pipelining ANSWER: B

1. Status register is also called as .
	1. accumulator B. stack C. counter D. flags ANSWER: D
2. Which is not an operand?
	1. Variable B. Register C. Memory location D. Assembler ANSWER: D
3. Which is not part of the execution unit (EU)?
	1. Arithmetic logic unit (ALU) B. Clock

C. General registers D. Flags ANSWER: B

1. Which of the following is not an 8086/8088 general-purpose register?
	1. Code segment (CS) B. Data segment (DS)

C. Stack segment (SS) D. Address segment (AS) ANSWER: D

1. A 20-bit address bus allows access to a memory of capacity
	1. 1 MB B. 2 MB C. 4 MB D. 8 MB ANSWER: A
2. Which microprocessor accepts the program written for 8086 without any changes? A. 8085 B. 8086 C. 8087 D. 8088

ANSWER: D

1. Which group of instructions do not affect the flags?
	1. Arithmetic operations B. Logic operations

C. Data transfer operations D. Branch operations

ANSWER: C

1. The main concerns of the are to define a flexible set of commands

A. memory interface B. peripheral interface

C. both (A) and (B) D. control interface

ANSWER: A

1. Primary function of memory interfacing is that the should be able to read from and write into register

A. multiprocessor B. microprocessor

C. dual Processor D. coprocessor

ANSWER: B

1. To perform any operations, the Mp should identify the

A. register B. memory C. interface D. system

ANSWER: A

1. The Microprocessor places address on the address bus

A. 4 bit B. 8 bit C. 16 bit D. 32 bit

ANSWER: C

1. 57. The Microprocessor places 16 bit address on the add lines from that address by register should be selected

A. address B. one C. two D. three

ANSWER: B

1. The of the memory chip will identify and select the register for the EPROM

A. internal decoder B. external decoder C. address decoder D. data decoder ANSWER: A

1. Microprocessor provides signal like to indicate the read operatio

A. LOW B. MCMW C. MCMR D. MCMWR ANSWER: C

1. 60. To interface memory with the microprocessor, connect register the lines of the address bus must be added to address lines of the chip.

A. single B. memory C. multiple D. triple

ANSWER: B

1. 61. The remaining address line of bus is decoded to generate chip select signal

A. data B. address C. control bus D. both (a) and (b) ANSWER: B

1. ------- generate interrupt signal to microprocessor and receive acknowledge

A. priority resolver B. control logic

C. interrupt request register D. interrupt register

ANSWER: B

1. The pin is used to select direct command word

A. A0 B. D7-D6 C. A12 D. AD7-AD6

ANSWER: A

1. The is used to connect more microprocessor

A. peripheral device B. cascade C. I/O devices D. control unit

ANSWER: B

1. 8086 and 8088 contains transistors

A. 29000 B. 24000 C. 34000 D. 54000

ANSWER: A

1. ALE stands for

A. address latch enable B. address level enable

C. address leak enable D. address leak extension

ANSWER: A

1. What is DEN?

A. direct enable B. data entered C. data enable D. data encoding

ANSWER: C

1. In 8086, Example for Non maskable interrupts are .

A. TRAP B. RST6.5 C. INTR D. RST6.6

ANSWER: A

1. In 8086 the overflow flag is set when .

A. the sum is more than 16 bits.

B. signed numbers go out of their range after an arithmetic operation.

C. carry and sign flags are set.

D. subtraction

ANSWER: B

1. In 8086 microprocessor the following has the highest priority among all type interrupts?

A. NMI B. DIV 0 C. TYPE 255 D. OVER FLOW

ANSWER: A

1. Status register is also called as .

A. accumulator B. stack C. counter D. flags

ANSWER: D

1. Which microprocessor has multiplexed data and address lines?

A. 8086 B. 80286 C. 80386 D. Pentium

ANSWER: A

**UNIT.IV – MICROCONTROLLER -8051**

1. 8051 microcontrollers are manufactured by which of the following companies?
a) Atmel b) Philips c) Intel d) All of the mentioned

Answer: d

1. AT89C2051 has RAM of:
a) 128 bytes b) 256 bytes c) 64 bytes d) 512 bytes

Answer: a

1. 3. 8051 series has how many 16 bit registers?
a) 2 b) 3 c) 1 d) 0

Answer: a

1. When 8051 wakes up then 0x00 is loaded to which register?
a) PSW b) SP c) PC d) None of the mentioned

Answer: c

1. When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected?

a) PSW b) SP c) DPTR d) PC

Answer: a

1. How are the status of the carry, auxiliary carry and parity flag affected if the write instruction MOV A,#9C, ADD A,#64H

a) CY=0,AC=0,P=0 b) CY=1,AC=1,P=0 c) CY=0,AC=1,P=0 d) CY=1,AC=1,P=1

 Answer: b

1. How are the bits of the register PSW affected if we select Bank2 of 8051?

a) PSW.5=0 and PSW.4=1 b) PSW.2=0 and PSW.3=1

c) PSW.3=1 and PSW.4=1 d) PSW.3=0 and PSW.4=1

Answer: d

1. If we push data onto the stack then the stack pointer

a) increases with every push b) decreases with every push

c) increases & decreases with every push d) none of the mentioned

Answer: a

1. On power up, the 8051 uses which RAM locations for register R0- R7

a) 00-2F b) 00-07 c) 00-7F d) 00-0F

Answer: b

1. How many bytes of bit addressable memory is present in 8051 based microcontrollers?

a) 8 bytes b) 32 bytes c) 16 bytes d) 128 bytes

Answer: c

1. 8051 is \_\_\_\_\_\_\_\_ microcontroller.

a). 4-bit b). 8-bit c). 16-bit d). All of the above

Answer : b

1. In Which year, Intel introduced 8051 microcontroller?

a) 1975 b) 1979 c)1981 d) 1985

Answer : c

1. Which of the following is Features of 8051 Microcontroller?

a) 16-bit program counter and data pointer b) Four 8-bit ports
c) Three internal and two external Interrupts d) All of the above

Answer : d

1. 8051 Microcontroller has 4KB bytes on-chip program memory?
2. TRUE b)FALSE c)Can be true or false d)Can not say

Answer : a

1. 8051 Microcontroller has ?
2. 8-bit unidirectional address bus b)16-bit unidirectional address bus

c) 8-bit bidirectional address bus d)16-bit bidirectional address bus

Answer : b

1. How much I/O pins 8051 has?

a) 4 b) 8 c) 16 d)32

Answer :d

1. 8031 microcontroller is another member of the 8051 family.

a) TRUE b) FALSE c)Can be true or false d)Can not say

Answer :a

1. 8051 Microcontroller has Four register banks?

a) Yes b)No c)Can be yes or no d)Can not say

Answer :a

1. Which port does not represent quasi-bidirectional nature of I/O ports in accordance to the pin configuration of 8051 microcontroller?

a. Port 0 (Pins 32-39) b. Port 1 (Pins 1-8)
c. Port 2 (Pins 21-28) d. Port 3 (Pins 10-17)

**ANSWER: a.**

1. Which memory allow the execution of instructions till the address limit of 0FFFH especially when the External Access (EA) pin is held high?

a. Internal Program Memory b. External Program Memory
c. Both a & b d. None of the above

**Answer: a.**

1. Which output control signal is activated after every six oscillator periods while fetching the external program memory and almost remains high during internal program execution ?

a. ALE b. PSEN c. EA d. All of the above

**Answer: b.**

### **Which is not the feature of 16-bit microcontroller?**

a)Large program & data memory spaces b)High speed

c)I/O Flexibility d) Limited Control Applications

**Answer:d**

### **Which is false about microcontroller?**

1. Microcontrollers are used to execute a single task within an application.
2. It consists of CPU, RAM, ROM, I/O ports.
3. Its power consumption is high because it has to control the entire system.
4. It is built with CMOS technology

Answer c

### **Unlike microprocessors, microcontrollers make use of batteries because they have:**

### **high power dissipation b)low power consumption**

### **c)low voltage consumption d)low current consumption**

Answer b

### **What is the order decided by a processor or the CPU of a controller to execute an instruction?**

1. decode, fetch, execute
2. execute, fetch, decode
3. fetch, execute, decode
4. fetch, decode, execute

Answer d

### **How are the performance and the computer capability affected by increasing its internal bus width?**

1. It increases and turns better b)It decreases

c)Remains the same d) Internal bus width doesn’t affect the performance in any way

Answer a

### **How many bytes of bit addressable memory is present in 8051 based microcontrollers?**

1. 8 bytes b)32 bytes c)16 bytes d)128 bytes

Answer c

### **How does the microcontroller communicate with the external peripherals / memory?**

1. via I/O ports b)via register arrays c)via memory d)all of the above

Answer a

### **What is the file extension is used to load in a microcontroller to execute an instruction?**

1. .doc b).c c).txt d).hex

Answer d

### **When the microcontroller execute some arithmetic operations, then the flag bit of which register are affected ?**

1. PSW b)SP c)DPTR d)PC

Answer : **a**

### **8051 microcontroller is designed by Intel in?**

1. 1980 b)1981 c)1982 d)1983

Answer : **b**

### **Which operations are performed by stack pointer during its incremental phase?**

1. Push b)Pop c)Return d)All of the above

Answer : **a**

### **Which of the following register usually store the output generated by ALU in several arithmetic and logical operations?**

1. Special Function Register b)Timer Register

c)Accumulator d)Stack Pointer

Answer : **c**

### **8051 series has how many 16 bit registers?**

1. 2 b)3 c)1 d)0

Answer : **a**

### **Which IO Port can be used for higher address byte with addresses A8-A15?**

1. PORT1 b)PORT0 c)PORT3 d)PORT2

Answer : **d**

1. How does the processor respond to an occurrence of the interrupt?

a. By Interrupt Service Subroutine b. By Interrupt Status Subroutine
c. By Interrupt Structure Subroutine d. By Interrupt System Subroutine

Answer: a

1. Which address / location in the program memory is supposed to get occupied when CPU jump and execute instantaneously during the occurrence of an interrupt ?

a. Scalar b. Vector c. Register d. All of the above

**Answer: b.**

1. Which location specify the storage / loading of vector address during the interrupt generation?

a. Stack Pointer b. Program Counter c. Data Pointer d. All of the above

**Answer: b**

1. Which among the below mentioned reasons is / are responsible for the generation of Serial Port Interrupt ?

a) Overflow of timer/counter 1 b) High to low transition on pin INT1
c) High to low transition on pin INT0 d) Setting of either TI or RI flag

Codes :
a. A & B
b. Only B
c. C& D
d. Only D

**Answer: d.**

1. How many machine cycle/s is / are executed by the counters in 8051 in order to detect '1' to '0' transition at the external pin?

a. One b. Two c. Four d. Eight

**Answer: b.**

1. Which among the below mentioned sequence of program instructions represent the correct chronological order for the generation of 2kHz square wave frequency?

1. MOV TMOD, 0000 0010 B
2. MOV TL0, # 06H
3. MOV TH0, # 06H
4. SETB TR0
5. CPL p1.0
6. ORG 0000H

a. 6, 5, 2, 4, 1, 3
b. 6, 1, 3, 2, 4, 5
c. 6, 5, 4, 3, 2, 1
d. 6, 2, 4, 5, 1, 3

**Answer: b.**

1. What is the maximum delay generated by the 12 MHz clock frequency in accordance to an auto-reload mode (Mode 2 ) operation of the timer?

a. 125 μ s b. 250 μ s c. 256 μ s d. 1200 μ s

**Answer: c.**

1. Why is it not necessary to specify the baud rate to be equal to the number of bits per second ?

a) Because each bit is preceded by a start bit & followed by one stop bit
b) Because each byte is preceded by a start byte & followed by one stop byte
c) Because each byte is preceded by a start bit & followed by one stop bit
d) Because each bit is preceded by a start byte &followed by one stop byte

**Answer: c**

1. What does the symbol '#' represent in the instruction MOV A, #55H ?

a. Direct data type b. Indirect data type
c. Immediate data type d. Indexed data type

**Answer: c.**

1. Which instruction should be adopted for moving an accumulator to the register
from the below mentioned mnemonics?

a. MOV A, Rn b. MOV A, @ Ri c. MOV Rn, A d. MOV direct, A

**Answer: c.**

1. What does the instruction XCHD A, @Ri signify during the data transfer in the program execution ?

a. Exchange of register with an accumulator
b. Exchange of direct byte with an accumulator
c. Exchange of indirect RAM with an accumulator
d. Exchange of low order digit indirect RAM with an accumulator

Answer: d.
2. Which flag allow to carry out the signed as well as unsigned addition and subtraction operations ?

a. CY b. OV c. AC d. F0

Answer: b
3. How many bytes are supposed to get occupied while subtracting indirect RAM from an accumulator along with borrow under the execution of SUBB A, @Ri?

a. 1 b. 2 c. 3 d. 4
 Answer: a
4. What can be the oscillator period for the multiplication operation of A & B in accordance to 16-bit product especially in B : A registers?

a. 12 b. 24 c. 36 d. 48

Answer: d
5. Which form of instructions also belong to the category of logical instructions in addition to bitwise logical instructions?

a. Single-operand instructions b. Rotate instructions
c. Swap instructions d. All of the above

**Answer: d.**

1. Which rotate instruction/s has an ability to modify CY flag by moving the bit-7 & bit-0 respectively to an accumulator?

a. RR & RL b. RLC & RRC c. RR & RRC d. RL & RLC

Answer: b
2. Which among the single operand instructions complement the accumulator without affecting any of the flags ?

a. CLR b. SETB c. CPL d. All of the above

Answer: c

1. What is the status of stack pointer for the execution of PUSH and POP operations ?

a. It gets post-decremented for PUSH & pre-incremented for POP
b. It gets pre-incremented for PUSH & post-decremented for POP
c. It gets pre-incremented for PUSH as well as POP
d. It gets post-decremented for PUSH as well as POP
Answer: b.
2. Which condition approve to prefer the EPROM/ROM versions for mass production in order to prevent the external memory connections?

a. size of code < size of on-chip program memory
b. size of code > size of on-chip program memory
c. size of code = size of on-chip program memory
d. none of the above

Answer: a.

1. The microcontrollers are used in \_\_\_\_\_\_\_\_\_\_\_\_

a) Computers, laptops, televisions b)Printers, refrigerators

c) Microwave owens d)All of the above

Answer: d

1. The speed of the microcontrollers are \_\_\_\_\_\_\_\_\_\_\_

a)High b)Slow c)Very high d)Better

Answer: b

1. How many of microcontrollers are there based on bits?

a)One b)Two c)Three d)Four

Answer:c

1. How many of microcontrollers are there based on instruction set?

a)One b)Two c)Three d)Four

Answer: b

1. The 8-bit microcontrollers are used to execute \_\_\_\_\_\_\_\_\_

a)Arithmetic operations only b)Logical operations only

 c) Both a and b d)None of the above

Answer: c

1. \_\_\_\_\_\_\_\_\_\_\_\_ is an example of 16 bit microcontroller

a) 8031 microcontrolle b)8051 microcontroller

c)8096 microcontroller d)None of the above

Answer: c

**UNIT :V INTERFACING DEVICES**

1. How many pins does the 8255 PPI IC contains?
2. 24
3. 20
4. 32
5. 40

Answer: d

1. In which mode do all the Ports of the 8255 PPI work as Input-Output units for data transfer?
2. BSR mode
3. Mode 0 of I/O mode
4. Mode 1 of I/O mode
5. Mode 2 of I/O mode

Answer: b

1. Which of the following pins are responsible for handling the on the Read Write control logic unit of the 8255 PPI?
2. CS'
3. RD'
4. WR'
5. 2ALL of the above

Answer: d

1. In which of the following modes is the 8255 PPI capable of transferring data while handshaking with the interfaced device?
2. BSR mode
3. Mode 0 of I/O mode
4. Mode 1 of I/O mode
5. Mode 2 of I/O mode

Answer: c

1. How many bits of data can be transferred between the 8255 PPI and the interfaced device at a time? or What is the size of internal bus of the 8255 PPI?
2. 16 bits
3. 12 bits
4. 8 bits
5. None of the above

Answer: c

1. Which port of the 8255 PPI is capable of performing the handshaking function with the interfaced devices?
2. Port A
3. Port B
4. Port C
5. All of the above

Answer: c

1. In cascaded mode, the number of vectored interrupts provided by 8259A is
a) 4
b) 8
c) 16
d) 64
Answer: d
2. When the PS(active low)/EN(active low) pin of 8259A used in buffered mode, then it can be used as a
a) input to designate chip is master or slave
b) buffer enable
c) buffer disable
d) none

Answer: b
9. When non-specific EOI command is issued to 8259A it will automatically
a) set the ISR
b) reset the ISR
c) set the INTR
d) reset the INTR
Answer: b

10. In the application where all the interrupting devices are of equal priority, the mode used is
a) automatic rotation
b) automatic EOI mode
c) specific rotation
d) EOI
Answer: a

11. In the I/O mode, the 8255 ports work as
a) reset pins
b) set pins
c) programmable I/O ports
d) only output ports
Answer: c

12. In BSR mode, only port C can be used to

a) set individual ports
b) reset individual ports
c) set and reset individual ports
d) programmable I/O ports
Answer: c
13. The feature of mode 0 is
a) any port can be used as input or output
b) output ports are latched
c) maximum of 4 ports are available
d) all of the mentioned
Answer: d

14. The strobed input/output mode is another name of
a) mode 0
b) mode 1
c) mode 2
d) none
Answer: b
15. If the value of the pin STB (Strobe Input) falls to low level, then
a) input port is loaded into input latches
b) input port is loaded into output latches
c) output port is loaded into input latches
d) output port is loaded into output latches
Answer: a
16. The signal, SLCT in the direction of signal flow, OUT, indicates the selection of
a) Control word register
b) CPU
c) Printer
d) Ports
Answer: c
17. The pulse width of the signal INIT at the receiving terminal must be more than
a) 10 microseconds
b) 20 microseconds
c) 40 microseconds
d) 50 microseconds

Answer: d
18. The signals that are provided to maintain proper data flow and synchronization between the data transmitter and receiver are
a) handshaking signals
b) control signals
c) input signals
d) none
Answer: a
19. The feature of mode 2 of 8255 is
a) single 8-bit port is available
b) both inputs and outputs are latched
c) port C is used for generating handshake signals
d) all of the mentioned
Answer: d

20. Programmable communication interface is used -------

 a) Serial data transmission

 b) parallel data transmission

 c) multi data transmission

 d) none of these

Answer: a

21. Identify the programmable interval timer from the following.

 a) 8252

 b) 8253

 c) 8279

 d) 8275

Answer: b

22. Intel’s programmable ------device (8253) facilitates the generation of accurate time delays.

 a) counter

 b) timer

 c) both a & b

 d) none of these

Answer: c

23 The programmable timer devices(8253) contains three independent -------------------

 a) 8

 b) 16

 c) 20

 d) 32

Answer: b

24. The 8-bit ----- data buffer interfaces internal circuit of 8253 to microprocessor.

 a) unidirectional

 b) single

 c) bidirectional

 d) none

Answer: c

25. The three counter available in 8253 are independent of each other in operation , but they are ------ to each other in organization.

 a) Similar

 b) Opposite

 c) Identical

 d) Common

Answer: c

26. The total number of modes the 8253 can work------

 a) 4

 b) 6

 c) 8

 d) 12

Answer: b

27. In this mode, the 8253 can be used as a ------- wave rate generator.

 a) Sine wave

 b) Cosine wave

 c) Square wave

 d) All of these

Answer: c

28. The I/O section is enabled only if CS is ---------

 a)High

 b) Low

 c) Very high

 d) very low

Answer: b

29. The GATE signal is ------- and should be -------- for normal counting

 a) Active low, low

 b) Normal , Normal

 c) Active high,high

 d) none

Answer: c

30. The specility of the 8253 counter is that they can be easily read on line without disturbing the ----- input to the counter.

 a) GATE

 b) CLK

 c) OUT

 d) WR

Answer: b

31. In direct memory access mode, the data transfer takes place
a) directly
b) indirectly
c) directly and indirectly
d) none of the mentioned
Answer: a
32. In 8257 (DMA), each of the four channels has
a) a pair of two 8-bit registers
b) a pair of two 16-bit registers
c) one 16-bit register
d) one 8-bit register
Answer: b
33. The common register(s) for all the four channels of 8257 is
a) DMA address register
b) Terminal count register
c) Mode set register and status register
d) None of the mentioned
Answer: c
34. The IOR (active low) input line acts as output in
a) slave mode
b) master mode
c) master and slave mode
d) none of the mentioned
Answer: b
35. The IOW (active low) in its slave mode loads the contents of a data bus to
a) 8-bit mode register
b) upper/lower byte of 16-bit DMA address register
c) terminal count register
d) all of the mentioned
Answer: d

36. The pin that disables all the DMA channels by clearing the mode registers is
a) MARK
b) CLEAR
c) RESET
d) READY
Answer: c
37. The pin that requests the access of the system bus is
a) HLDA
b) HRQ
c) ADSTB
d) None of the mentioned
Answer: b
38. The pin that is used to write data to the addressed memory location, during DMA write operation is
a) MEMR (active low)
b) AEN
c) MEMW (active low)
d) IOW (active low)
Answer: c
39. The register that stores all the interrupt requests in it in order to serve them one by one on a priority basis is
a) Interrupt Request Register
b) In-Service Register
c) Priority resolver
d) Interrupt Mask Register
Answer: a
40. The register that stores the bits required to mask the interrupt inputs is
a) In-service register
b) Priority resolver
c) Interrupt Mask register
d) None
Answer: c
41. The interrupt control logic
a) manages interrupts
b) manages interrupt acknowledge signals
c) accepts interrupt acknowledge signal
d) all of the mentioned
Answer: d
42. In a cascaded mode, the number of vectored interrupts provided by 8259A is
a) 4
b) 8
c) 16
d) 64
Answer: d
43.When the PS(active low)/EN(active low) pin of 8259A used in buffered mode, then it can be used as a
a) input to designate chip is master or slave
b) buffer enable
c) buffer disable
d) none
Answer: b
44. In the application where all the interrupting devices are of equal priority, the mode used is
a) Automatic rotation
b) Automatic EOI mode
c) Specific rotation
d) EOI
Answer: a
45. Which of the following is not a mode of data transmission?
a) simplex
b) duplex
c) semi duplex
d) half duplex
Answer: c
46. In 8251A, the pin that controls the rate at which the character is to be transmitted is
a) TXC(active low)
b) TXC(active high)
c) TXD(active low)
d) RXC(active low)
Answer: a
47. TXD(Transmitted Data Output) pin carries serial stream of the transmitted data bits along with
a) start bit
b) stop bit
c) parity bit
d) all of the mentioned
Answer: d
48. The signal that may be used either to interrupt the CPU or polled by the CPU is
a) TXRDY(Transmitter ready)
b) RXRDY(Receiver ready output)
c) DSR(active low)
d) DTR(active low)
Answer: b
49. The register that stores the bits required to mask the interrupt inputs is

a) In-service register
b) Priority resolver
c) Interrupt Mask register
d) none
Answer: c
50. The interrupt control logic

a) manages interrupts
b) manages interrupt acknowledge signals
c) accepts interrupt acknowledge signal
d) all of the mentioned
Answer: d

51. 8251 contains …..bits control word register divided into two sections of …..bits each.

a. 16,8 b. 8,4 c. 32,16 d. None of these.

Answer: a

52. ………. register must be initialized before any use of 8251.

a. Command word register b. Control word register

 c. Mode word register d. Both a & c.

Answer: a

53. On 5 bits data transmission data must be represented by…….

a. LSB b. MSB c. Preceding 1 LSB d. Following 2 MSB

Answer: a

54. In asynchronous mode D7, D6 defines number of ………..bits.

a. Stop b. Parity c. Character length d. None of these

 Answer: a

55. ……………… status register is set if transmit buffer is empty

 a. TxRDY b. DTR c. CS d. None of these

Answer: a

56. Which is the programmable communication interface?

a. 8255 b. 8251 c. 8254 d. 8259

Answer: b

57. The communication between processor & 8251 can be done in ………mode only.

a. Parallel b. Serial c. Both a & b d. None of these

Answer: a

58. 8251 converts………..data for transmission to communicate with microprocessor.

a. Parallel to serial b. Serial to parallel c. Both a & b d. None of these

Answer: b

59. 8251 is a ……………..

 a. UART b. USART c. Programable interrupt controller d. Programable interval timer/counter

Answer: b

60. 8251 synchronous baud rate is……………..

a. 64K b. 19.2K c. 32K d. 12K

Answer: a